**Ex No: 05**

**Date: 17.10.2024**

**4-BIT UP/DOWN SYNCHRONOUS COUNTER USING D-FLIP FLOP**

**AIM:**

To design and implement a 4-bit Up/Down Synchronous Counter using Cadence Virtuoso 90nm CMOS technology**.**

**TOOLS REQUIRED:**

Cadence Virtuoso Analog Design Environment

**PROCEDURE:**

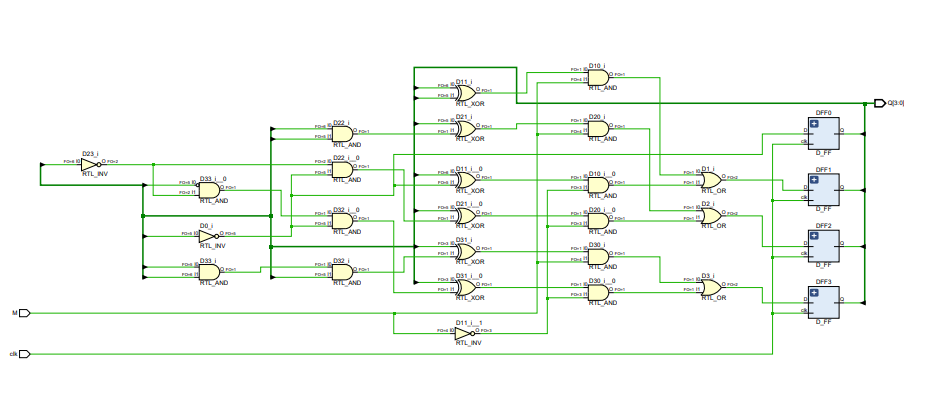
* + - * Open Virtuoso and create a new library with existing gpdk090nm technology.
      * File -> New -> Cellview -> Schematic
      * With the help of the circuit diagram, implement the D-Flip Flop using cmos by adding instances and connect the instances using wire
      * Add the source and ground to the required pins
      * Complete the circuit with the wireconnections
      * Launch ->ADE L
      * Choose Transient analysis

Set the stop time

Click on moderate

* + - * Select input and output pins from the design by clicking on the corresponding wires
      * Then run the simulation process to get the transient response
      * Thus, the pre layout simulation results are obtained.

**CIRCUIT DIAGRAM:**

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**Fig 5.1 Circuit diagram of 4 bit synchronous up/down counter**

**STATE DIAGRAM:**

A circular diagram of numbers and arrows

Description automatically generated

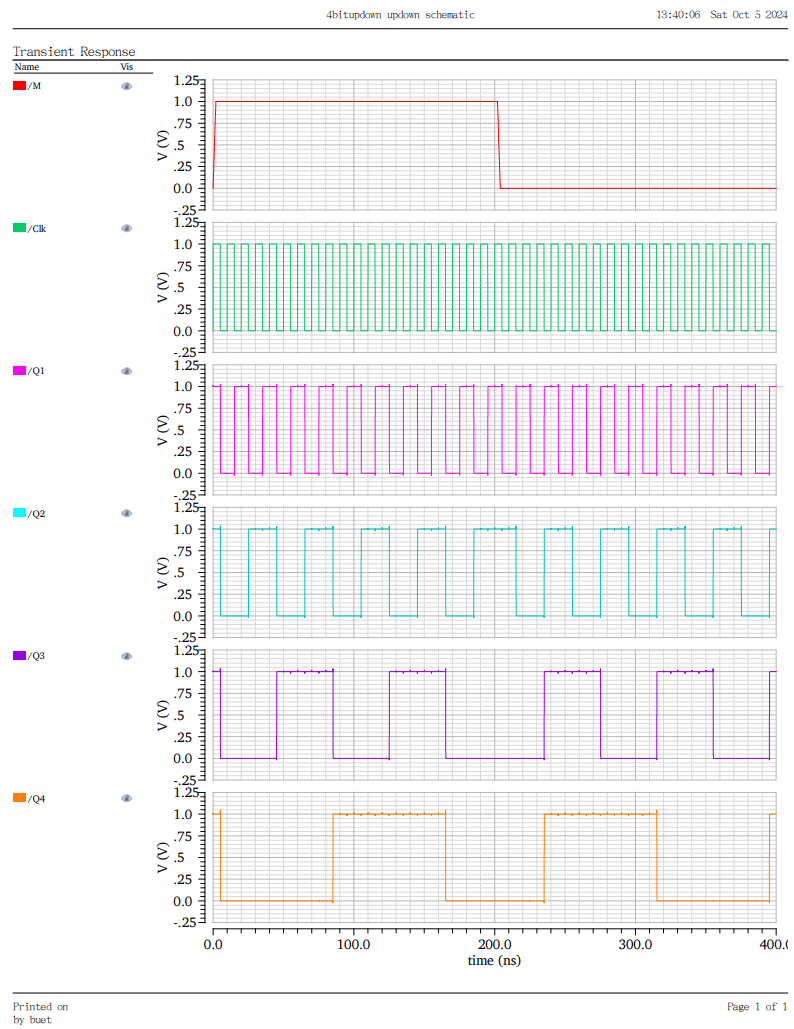
**Fig 5.2 State diagram of 4 bit synchronous up/down counter**

**TRANSIENT ANALYSIS:**

**A diagram of a computer

Description automatically generated**

**Fig 5.3 Schematic Diagram of 4 bit synchronous up/down counter**

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**Fig 5.4 Transient Analysis of 4 bit synchronous up/down counter**

**RESULT:**

Thus, the 4-bit synchronous up/down counter using D flipflop was implemented and verified using Cadence Virtuoso Analog Design Environment.